

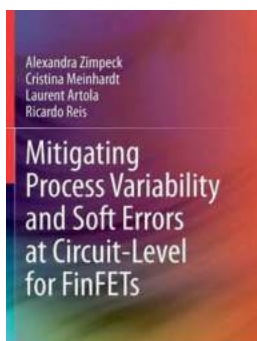
# Mitigating Process Variability And Soft Errors At Circuit Level For Finfets

Process variability and soft errors are significant challenges that the semiconductor industry faces in the advancement of technology. As integrated circuits continue to scale down in size, ensuring reliable performance becomes increasingly difficult. This article discusses the importance of mitigating process variability and soft errors at the circuit level, specifically for FinFETs.

## Understanding Process Variability

Process variability refers to the unavoidable, random variations that occur during the manufacturing process of integrated circuits. These variations can lead to inconsistencies in performance characteristics such as speed, power consumption, and reliability. With FinFET technology, the variability is even more pronounced due to the complex three-dimensional transistor structure.

One of the main causes of process variability is the lithography process, which determines the dimensions and placement of transistors on the silicon wafer. Small variations in the alignment or exposure during lithography can result in different transistor characteristics. Other sources of variability include the doping process, thin film deposition, and etching, among others.



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## Mitigating Process Variability and Soft Errors at Circuit-Level for FinFETs

by Alexandra Zimpeck (1st ed. 2021 Edition, Kindle Edition)

★★★★★ 5 out of 5

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To ensure reliable circuit operation, it is essential to identify and mitigate the effects of process variability. By understanding the sources and nature of the variability, designers can implement techniques to compensate and reduce its impact on circuit performance.

## **The Impact of Process Variability on FinFETs**

FinFETs have become a popular choice for advanced semiconductor technology due to their superior performance and scalability. However, their unique three-dimensional structure makes them more susceptible to process variability.

The variability in FinFETs can result in variations in threshold voltage, gate oxide thickness, and channel doping concentration. These variations can affect the performance and reliability of the circuits implemented using FinFETs.

The threshold voltage variation, for instance, can lead to variations in the transistor's on-state current, influencing the circuit's speed and power consumption. Variations in the gate oxide thickness can impact the reliability and leakage current of the transistor. The channel doping concentration variations can affect the transistor's sub-threshold characteristics, affecting its power consumption and performance.

## **Mitigating Process Variability at the Circuit Level**

Several techniques can be employed at the circuit level to mitigate the effects of process variability and ensure reliable operation of FinFET-based circuits.

## **1. Adaptive Circuit Design**

Adaptive circuit design techniques involve designing circuits that can adapt to process variations by dynamically adjusting their operating parameters. These techniques rely on circuit-level sensing and feedback mechanisms to continuously monitor and optimize circuit performance.

For example, adaptive body biasing can be employed to compensate for threshold voltage variations. By dynamically adjusting the body bias voltage, the threshold voltage of the transistor can be regulated, ensuring consistent performance across different process variations.

## **2. Statistical Design Methods**

Statistical design methods involve designing circuits that can tolerate a certain degree of process variability without compromising performance or reliability. These methods utilize statistical modeling and analysis techniques to understand and accommodate the variations within the design process.

Design techniques such as guardbanding and worst-case design allow for a margin of error in design specifications, ensuring that even under worst-case process variations, the circuit will still meet its performance and reliability requirements.

## **3. Redundancy and Error Detection Techniques**

Redundancy and error detection techniques can be employed to enhance the reliability of circuits by detecting and correcting errors caused by process variations. These techniques involve duplicating critical components or using error detection codes to identify and correct errors.

For example, redundant representations can be used to store critical data in multiple forms, mitigating the impact of errors caused by process variations on data integrity. Parity or error-correcting codes can be employed to detect and correct errors in data transmission.

## **Soft Errors and Their Mitigation**

In addition to process variability, soft errors pose another challenge in the design of reliable circuits. Soft errors are transient faults caused by energetic particles, such as cosmic rays or alpha particles, striking the semiconductor device and altering its state temporarily.

In FinFET-based circuits, the three-dimensional transistor structure increases the likelihood of charge collection from particle strikes, making them more susceptible to soft errors.

Several techniques can be adopted to mitigate the impact of soft errors on circuit performance:

### **1. Error-Correcting Codes**

Error-correcting codes can be applied to critical data storage or transmission to detect and correct errors caused by soft errors. These codes introduce redundancy in the data, enabling error detection and recovery.

### **2. Radiation-Hardened Designs**

Radiation-hardened designs involve incorporating features or materials that are less susceptible to radiation-induced soft errors. For example, using thick metal layers or dielectric materials with higher radiation-tolerance can improve circuit reliability.

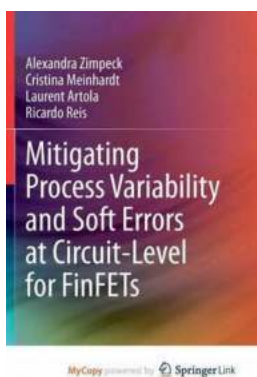
### 3. Error-Mitigating Architectures

Error-mitigating architectures involve designing circuits with built-in resilience and error-checking capabilities. For instance, triple modular redundancy (TMR) can be used to duplicate critical components and compare their outputs, reducing the probability of common-mode soft errors.

As semiconductor technology continues to advance, mitigating process variability and soft errors at the circuit level becomes increasingly crucial. FinFET-based circuits are particularly susceptible to these challenges due to their complex three-dimensional structure.

Designers can adopt various techniques at the circuit level to minimize the impact of process variability and soft errors. Adaptive circuit design, statistical design methods, redundancy, and error detection techniques all play a significant role in ensuring reliable circuit operation.

By understanding the sources and characteristics of process variability and employing mitigation techniques, designers can push the boundaries of semiconductor technology while maintaining the required performance, reliability, and resilience.



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This book evaluates the influence of process variations (e.g. work-function fluctuations) and radiation-induced soft errors in a set of logic cells using FinFET technology, considering the 7nm technological node as a case study. Moreover, for accurate soft error estimation, the authors adopt a radiation event generator tool (MUSCA SEP3), which deals both with layout features and electrical properties of devices. The authors also explore four circuit-level techniques (e.g. transistor reordering, decoupling cells, Schmitt Trigger, and sleep transistor) as alternatives to attenuate the unwanted effects on FinFET logic cells. This book also evaluates the mitigation tendency when different levels of process variation, transistor sizing, and radiation particle characteristics are applied in the design. An overall comparison of all methods addressed by this work is provided allowing to trace a trade-off between the reliability gains and the design penalties of each approach regarding the area, performance, power consumption, single event transient (SET) pulse width, and SET cross-section.

Michael Stevens

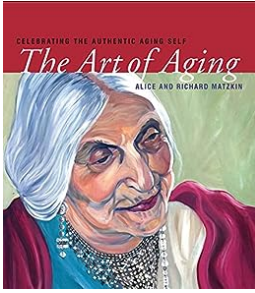
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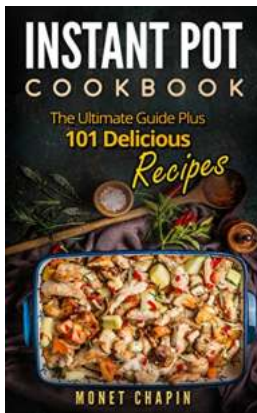
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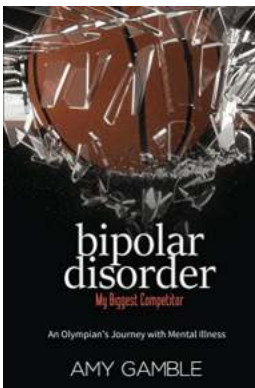
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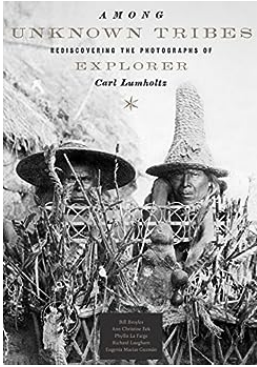
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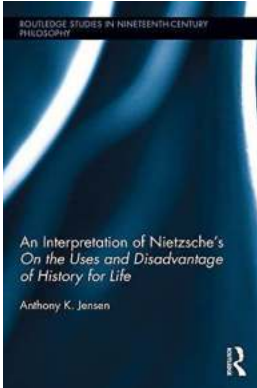
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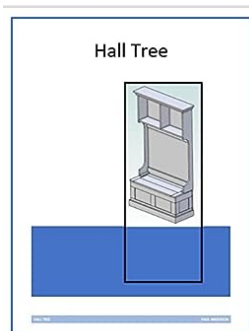
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